[0025] In some example embodiments, the conductive pattern may include an aluminum-containing material.

[0026] In some example embodiments, a width of the contact hole may be smaller than the width of the first opening, when measured in the specific direction.

[0027] According to some example embodiments of the inventive concepts, a semiconductor chip may include an integrated circuit on a substrate, a pad electrically connected to the integrated circuit, a lower insulating structure having a contact hole exposing the pad, and a conductive pattern including a contact portion filling the contact hole, a conductive line portion provided on the lower insulating structure to extend in a specific direction, and a bonding pad portion. The lower insulating structure may include a first region and a second region, the top surface thereof may be lower than the top surface of the first region, the first region may overlap the conductive pattern a plan view, the second region may be exposed by the conductive pattern, and the lower insulating structure a include a plurality of air gaps provided therein.

[0028] In some example embodiments, the semiconductor chip may further include an upper insulating structure having an opening exposing the bonding pad portion. The upper insulating structure may include an upper insulating layer covering the lower insulating structure and the conductive pattern, and a polymer layer on the upper insulating layer.

[0029] In some example embodiments, the upper insulating layer may be provided to directly cover a top surface of the second region.

[0030] In some example embodiments, the semiconductor chip may further include a barrier pattern interposed between the lower insulating structure and the conductive pattern. The conductive pattern may include an aluminum-containing material, and the barrier pattern may include Ti, TiN, or any combination thereof.

[0031] According to some example embodiments of the inventive concepts, a semiconductor package may include a package substrate, and a semiconductor chip provided on and electrically connected to the package substrate with a wire. The semiconductor chip may include first and second surfaces facing each other, the first surface facing the package substrate, a pad provided on the second surface, a lower insulating structure having a contact hole exposing the pad, a conductive pattern including a contact portion filling the contact hole, a conductive line portion provided on the lower insulating structure to extend in a specific direction, and a bonding pad portion in contact with the wire, and an upper insulating structure having an opening exposing the bonding pad portion. The lower insulating structure may be provided to have a recess region formed in an upper portion thereof, when viewed in a plan view, the recess region may not overlap the conductive pattern, and the lower insulating structure may include a plurality of air gaps formed therein.

[0032] In some example embodiments, the upper insulating structure may include an inorganic insulating layer covering the lower insulating structure and the conductive pattern and including a silicon-containing material, and a polymer layer on the inorganic insulating layer.

[0033] In some example embodiments, the inorganic insulating layer may be provided to directly cover side and bottom surfaces of the recess region.

[0034] In some example embodiments, the semiconductor chip further may include an integrated circuit electrically connected to the pad, and the integrated circuit may be electrically connected to the package substrate through the pad, the conductive pattern, and the wire.

[0035] In some example embodiments, the semiconductor chip may include a plurality of semiconductor chips, which are stacked, for example sequentially stacked on the package substrate, and each of which is electrically connected to the package substrate through the bonding pad portion and the

[0036] In some example embodiments, the lower insulating structure ay include a first lower insulating layer adjacent to the pad, a second lower insulating layer adjacent to the conductive pattern, and a third lower insulating layer interposed between the first and second lower insulating layers, and the air gaps may be provided in the second lower insulating layer.

[0037] According to some example embodiments of the inventive concepts, a method of fabricating a semiconductor chip may include forming a pad on a substrate, the pad being electrically connected to an integrated circuit, forming a lower insulating structure on the substrate to cover the pad, the lower insulating structure including a plurality of air gaps formed therein, patterning the lower insulating structure to form a contact hole exposing the pad, forming a conductive layer on the lower insulating structure to fill the contact hole, the conductive layer being formed using a physical vapor deposition process, and patterning the conductive layer to form a conductive pattern extending in a specific direction on the lower insulating structure. The conductive layer in the contact hole may have a first thickness in a direction substantially perpendicular to a top surface of the substrate and a second thickness in a direction substantially parallel to the top surface of the substrate, and the first thickness may be greater than the second thickness.

[0038] In some example embodiments, the forming of the lower insulating structure may include forming at least one lower insulating layer on the substrate, patterning the lower insulating layer to form a plurality of lower insulating patterns, the lower insulating patterns defining empty spaces therebetween, and forming an additional insulating layer on the lower insulating patterns to form air gaps from the empty spaces.

[0039] In some example embodiments, the conductive pattern may include a bonding pad portion, the method further may include forming an upper insulating structure on the conductive pattern, the upper insulating structure including an upper insulating layer covering the conductive pattern and a polymer layer on the upper insulating layer, and pattering the upper insulating structure to form an opening exposing the bonding pad portion.

[0040] In some example embodiments, the patterning of the conductive layer may include forming a recess region in an upper portion of the lower insulating structure, and when viewed in a plan view, the recess region may be formed to be not overlapped with the conductive pattern.

[0041] In some example embodiments, the conductive layer may include an aluminum-containing material, and the pattering of the conductive layer may include forming a photoresist pattern on the conductive layer, and performing a dry etching process on the conductive layer using the photoresist pattern as an etch mask.

BRIEF DESCRIPTION OF THE DRAWINGS

[0042] Example embodiments will be more clearly understood from the following brief description taken in conjunc-